

Fig. 17E

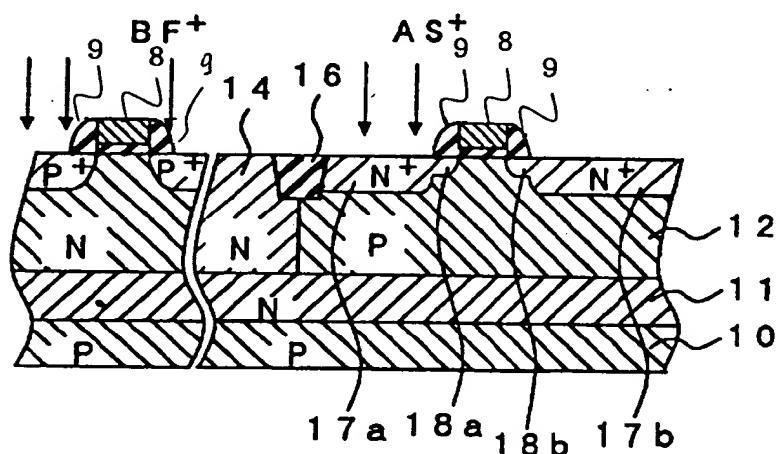


Fig. 17F

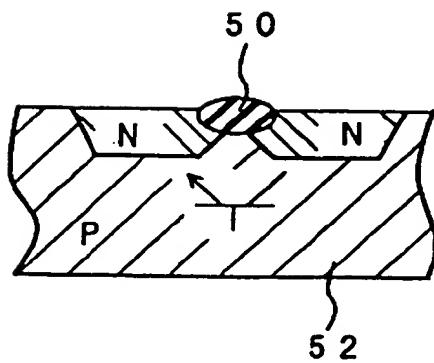


Fig. 1A
PRIOR ART

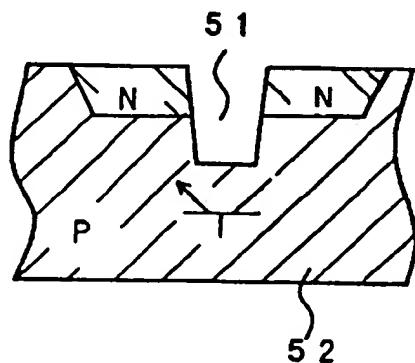


Fig. 1B
PRIOR ART

Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT
IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

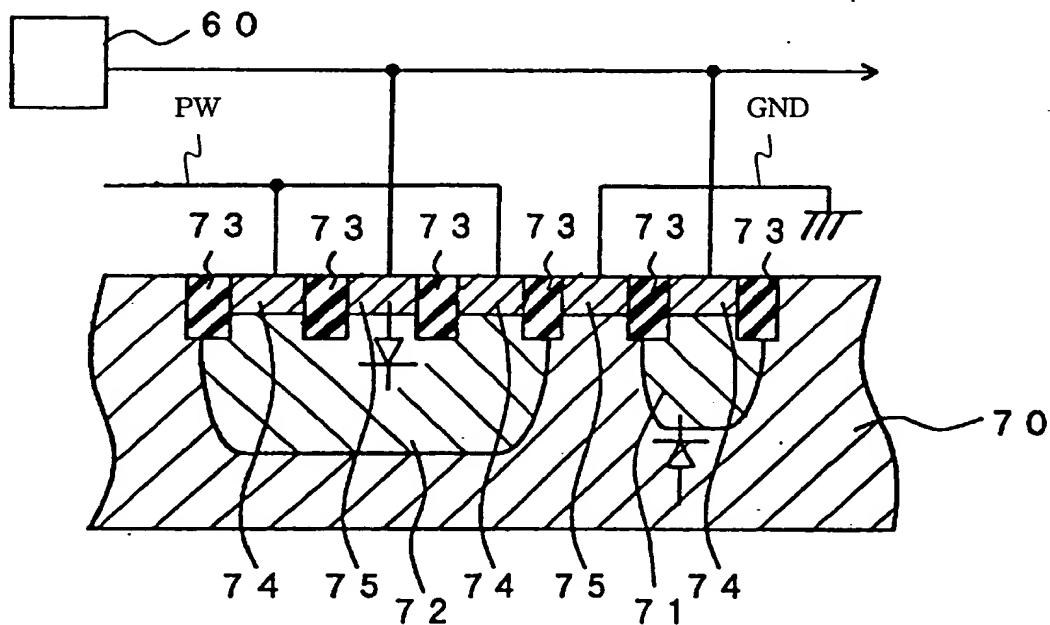


Fig. 2
PRIOR ART

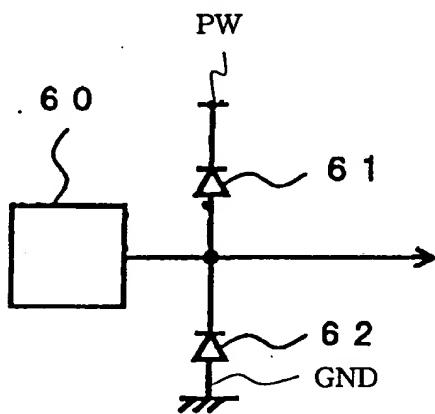


Fig. 3
PRIOR ART

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IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
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Inventor: Kaoru NARITA
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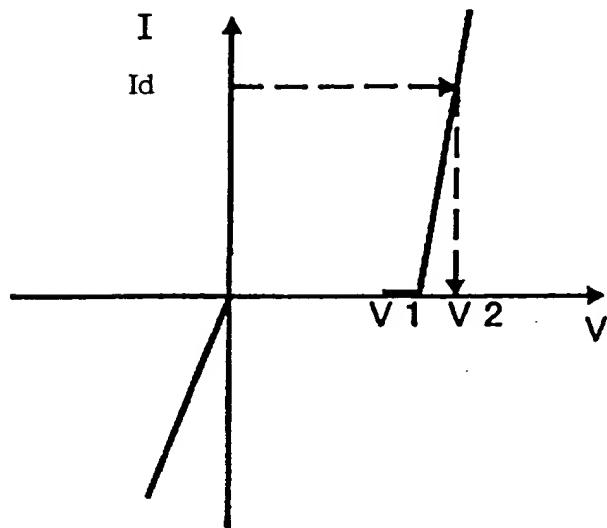


Fig. 4
PRIOR ART

**Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT
IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION**

Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

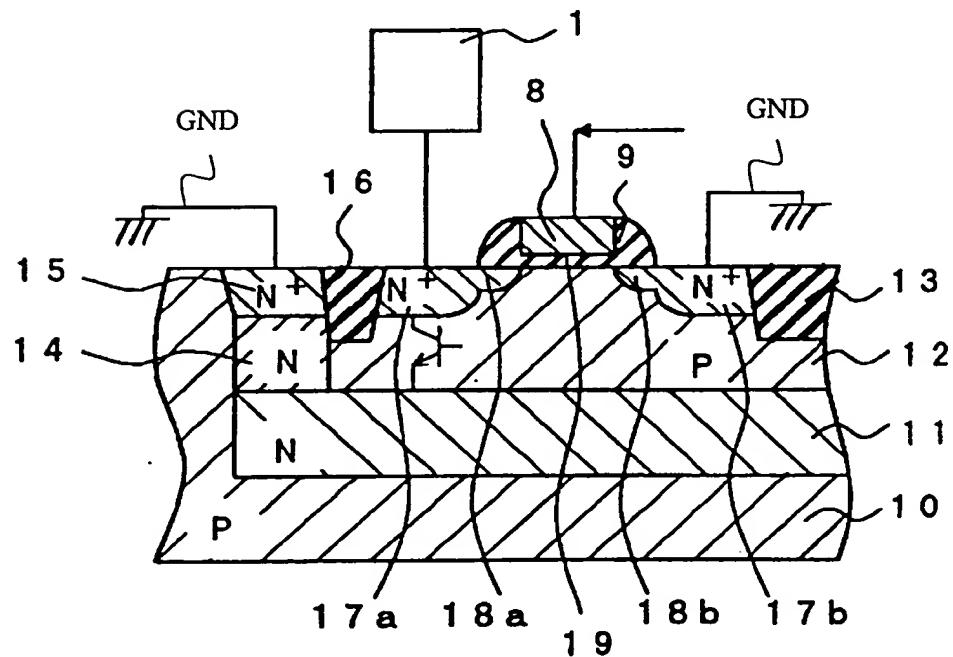


Fig. 5

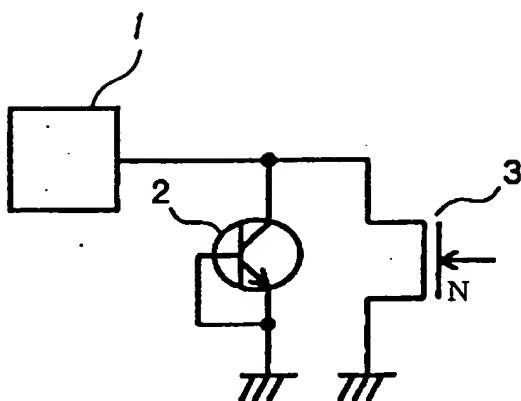


Fig. 6

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IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION**

Inventor: Kaoru NARITA
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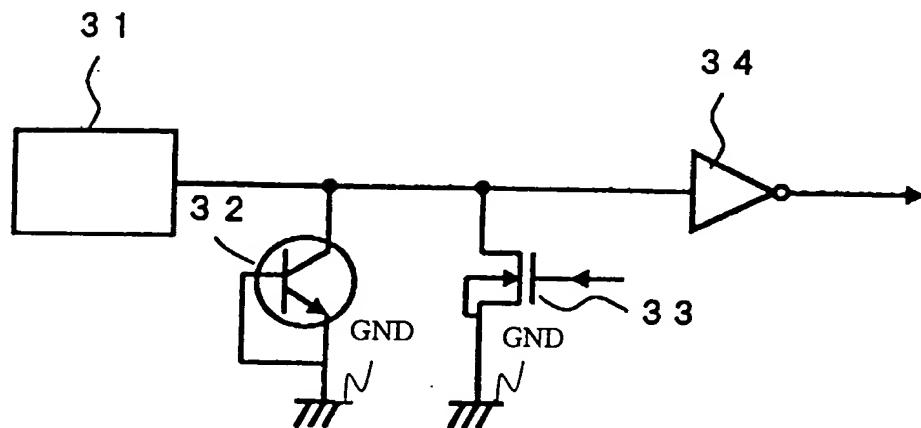


Fig. 15

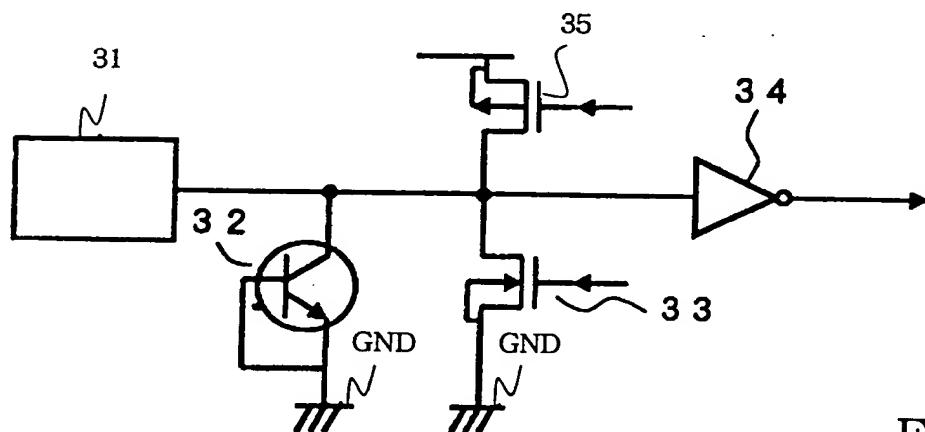


Fig. 16

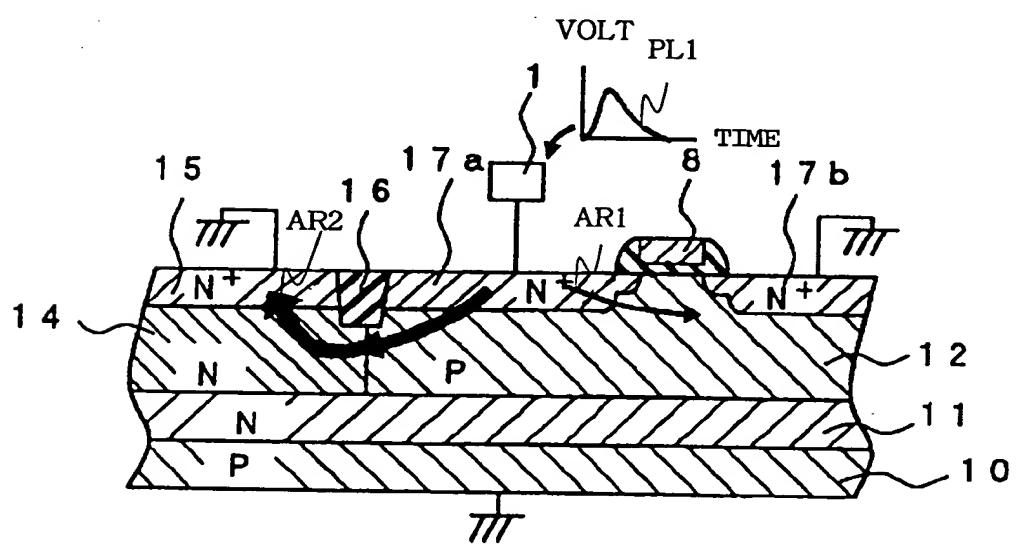


Fig. 7

**Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT
IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION**

Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

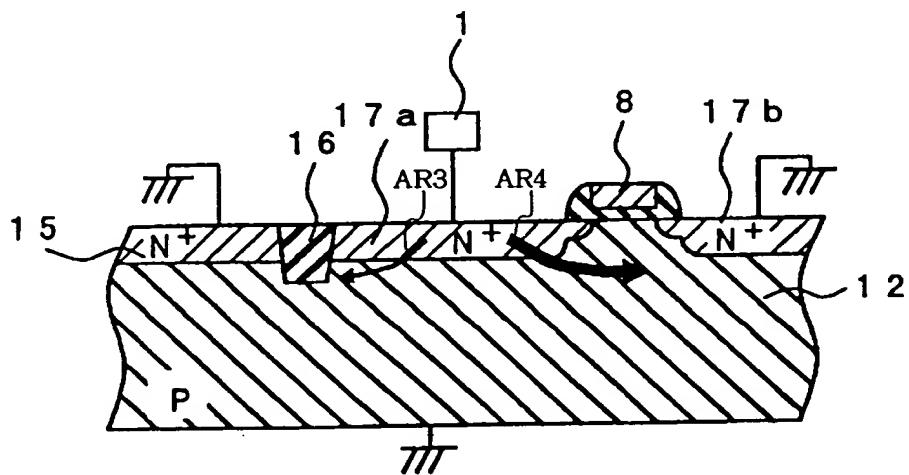


Fig. 8
PRIOR ART

Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT
IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

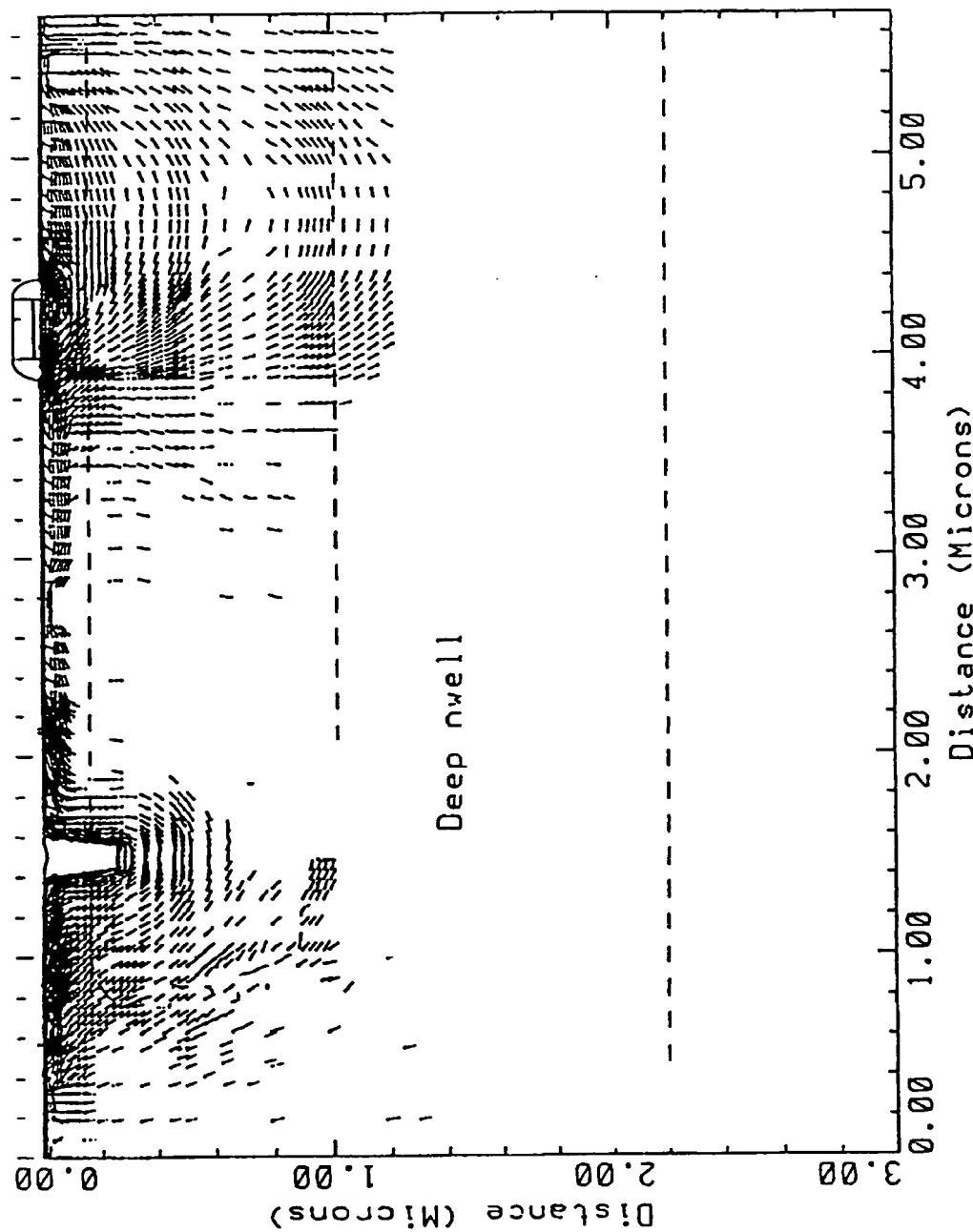


Fig. 9

Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT
IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

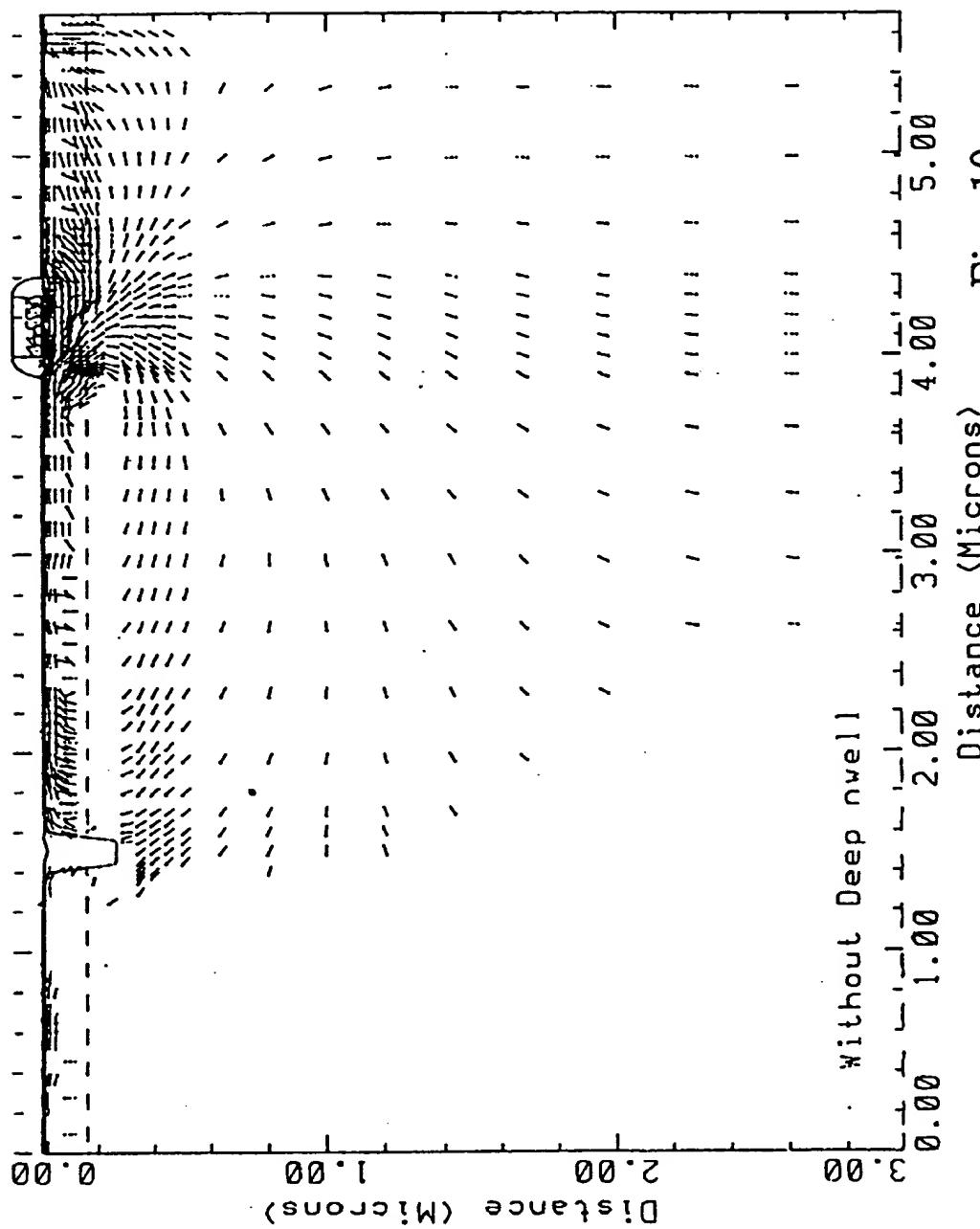


Fig. 10
PRIOR ART

Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT
IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

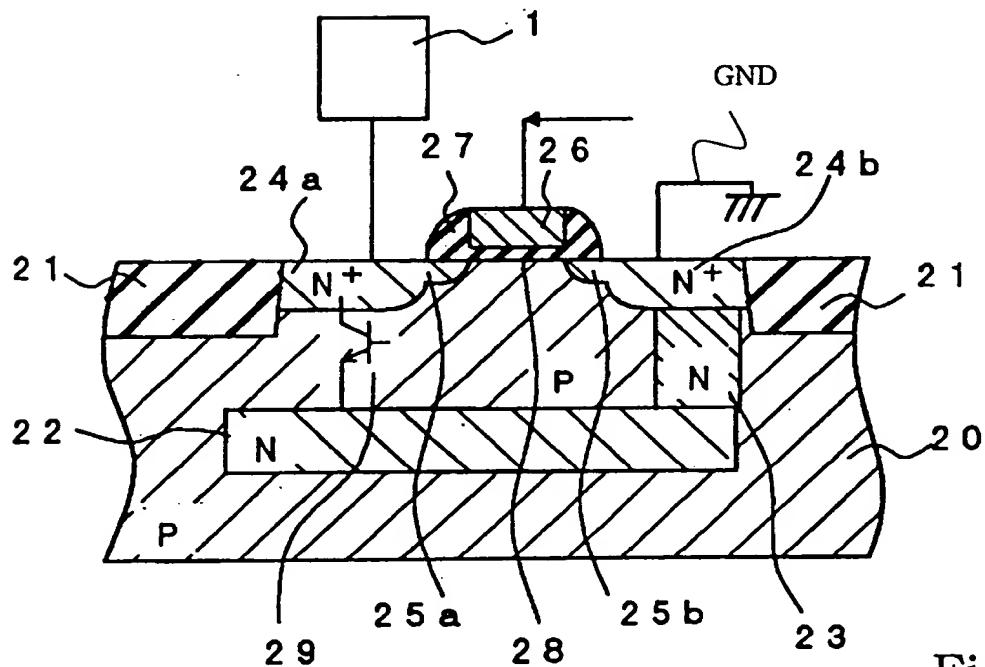


Fig. 11

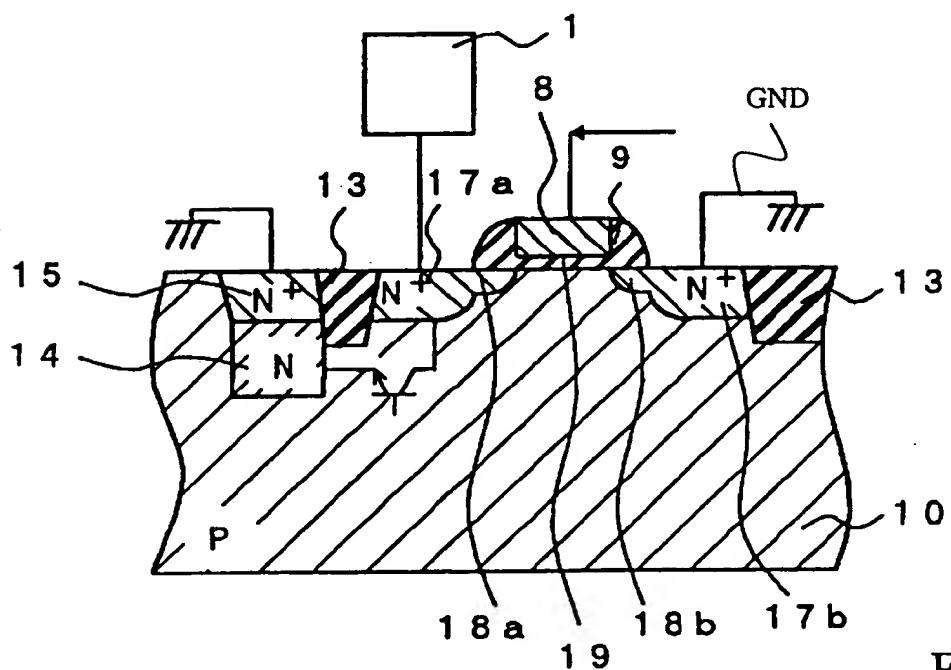


Fig. 12

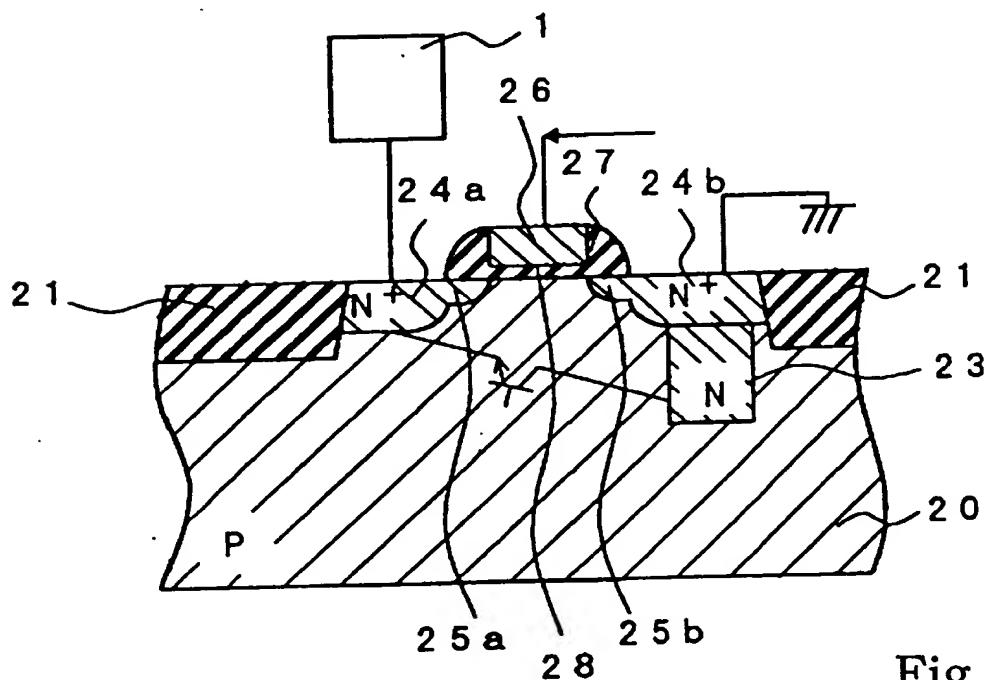


Fig. 13

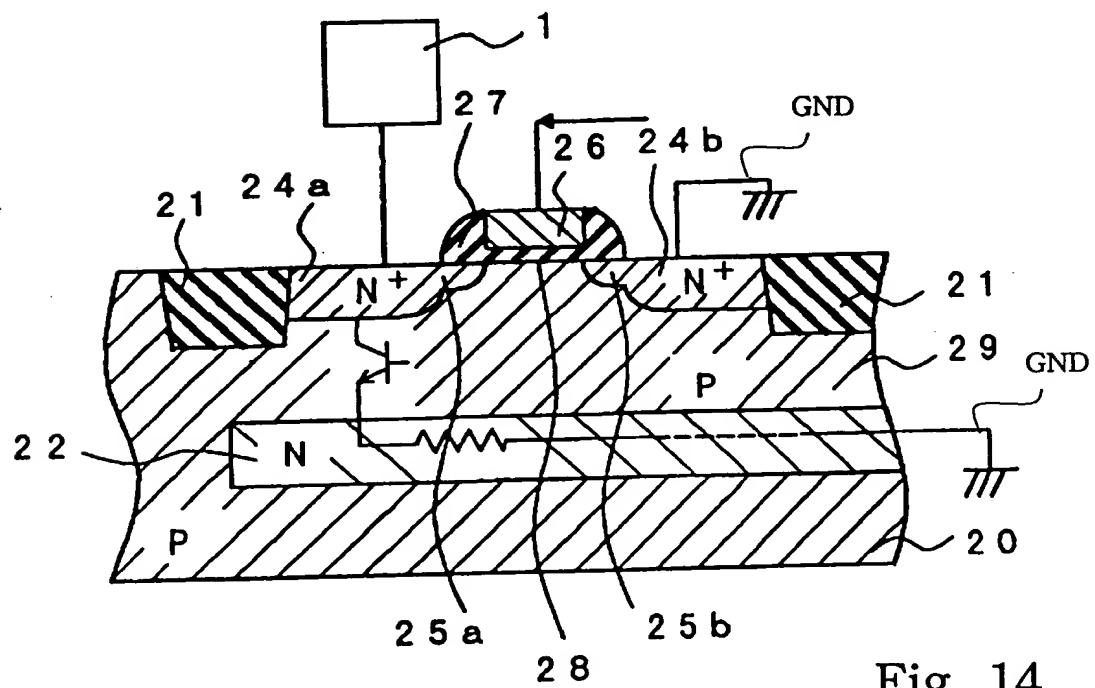


Fig. 14

Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT
IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING
STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

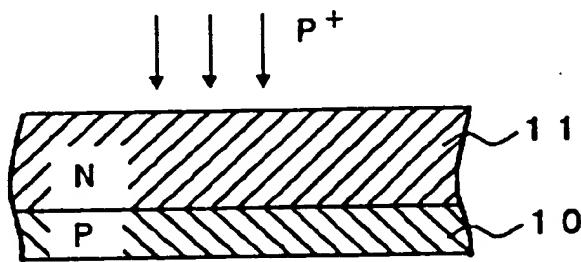


Fig. 17A

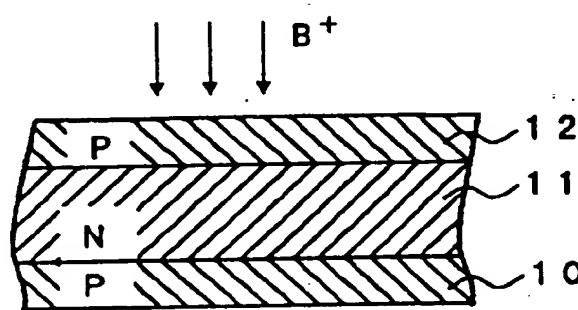


Fig. 17B

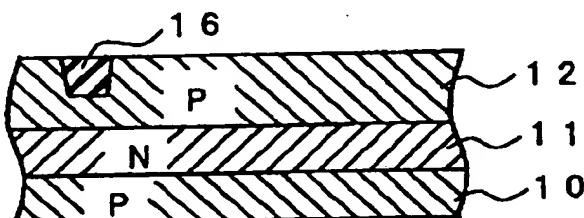


Fig. 17C

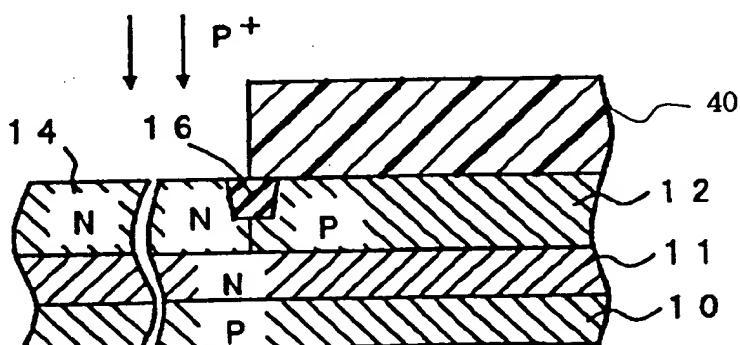


Fig. 17D